REMARKS

Claims 1-17 and 19-45 were pending in the application. By this paper, Applicant has cancelled Claims 8-17, 19 and 25 without prejudice, amended Claims 1, 20, 26, 32, 34, 35, 40, 42 and 43, and added new Claims 46-50. Accordingly, Claims 1-7, 20-24 and 26-50 are presented herein for examination.

General

Applicant thanks the Examiner for the detailed Office Action, which the Examiner clearly expended considerable effort preparing.

Claim Objections and Rejections under §112

Claims 43-45 were rejected under 35 U.S.C. §112 second paragraph (see Pars. 5-7 of the Office Action). By this paper, Applicant has amended Claim 43 to further clarify, but Applicant respectfully traverses the Examiner's rejection on lack of requisite antecedent basis. Specifically, the second limitation of the claim as previously presented reads:

"*receiving one or more inputs from a user for at least one customized parameter*..."

Applicant submits that this acts as the antecedent basis for the later recitation of the customized parameter. The recitation of the prototype description and extension logic description are then introduced for the first time, and hence do not require an antecedent basis.

Accordingly, Applicant submits that these amendments and arguments overcome the Examiner's rejections.

Section 102 Rejections

Applicant has herein cancelled all claims without prejudice that were rejected by the Examiner under Section 102, thereby rendering these rejections moot.

Section 103 Rejections

Regarding the Examiner's Section 103 rejections of Claims 1-7, 11-13, 15-17, 20-24, 26-31, 32-34, and 35-41 per the Office Action, Applicant provides the following responses.

Claims 11-13 and 15-17 – By this paper, Claims 11-13 and 15-17 are cancelled without prejudice, thereby rendering these rejections moot.

Claim 1 - By this paper, Applicant has amended independent Claim 1 to include limitations relating to (i) individual ones of said instruction types being included within at least one of 16-bit and 32-bit instruction words; and (ii) the act of creating a compressed instruction set comprises creating at least one compressed 14-bit instruction disposed within one of said 16-bit or 32 bit words. Support for these limitation are replete through Applicant's specification; see, *inter alia*, Fig. 2, page 11, lines 17-21, and page 14, lines 6-10 of Applicant's specification as filed.

Applicant respectfully submits that none of the cited art used as the basis for the Examiner's rejection teaches or suggests such limitations in any way. Applicant notes that in contrast to the Examiner's assertions regarding Killian (6,477,683) with respect to Claims 11-13 on page 20 of the Office Action, Killian respectfully does not in any way teach or suggest a 14-bit (or other integer) instruction coding as now recited in Claim 1. Rather, the portion of Killian cited by the Examiner as standing for this proposition (Col. 20, lines 31-34 of Killian) states:

> "*Alternatively or in conjunction therewith, a compiler-like tool checks if the user program uses bit-mask operations to insure that certain variables are never larger than certain limits. In this situation, the tool suggests to the search engine 106 a co-processor 98 using* ***data*** *types conforming to the user limits (for example, 12 bit or 20 bit or any other size integers).*" {Emphasis added}

In Killian, the user specifies data size limits; this is in now way suggestive of an instruction set architecture, or instruction encodings, which are based on those integers. Applicant submits that its 14-bit instruction encodings of the exemplary embodiment claimed in Claim 1 herein required

significant additional development and experimentation in order to achieve the benefits noted on pages 11-12 (starting at line 11 of page 11) of Applicant's specification as filed. An arbitrary choice of an integer value for an instruction coding would simply not work. But Killian does not even go so far as to teach an arbitrary or variable instruction set coding; rather, it only teaches a variable size **data** bit mask. Applicant respectfully submits that stretching this teaching to cover Applicant's claimed invention of Claim 1 using a purposely selected 14-bit instruction encoding would be highly specious at best.

Claims 20, 35 and 42 - By this paper, Applicant has amended Claim 20 to include limitations relating to the recited pipeline being operative to utilize said optimized instruction set without instruction translation. Support for these limitation are provided at, *inter alia*, page 5, lines 3-19 of Applicant's specification as filed (discussing deficiency of prior art including need to perform translate; see also discussion of prior art IBM Codepack in Applicant's specification, identifying disabilities of the prior art relating to instruction translation), and the detailed description portion of Applicant's specification which discloses at least one embodiment that does not require translation.

Applicant respectfully submits that none of the cited art used as the basis for the Examiner's rejection teaches or suggests such limitations in any way. Accordingly, the art cited by the Examiner cannot as a matter of law render Claim 20 as amended obvious, since not every limitation of the claim is present or suggested in such art.

Similar arguments apply to Claims 35 and 42 as amended herein.

Claim 26 - By this paper, Applicant has amended Claim 26 to include limitations relating to the recited 16-bit instructions from said plurality of 16-bit and 32-bit instructions being processed as 16-bit instructions, and 32-bit instructions from said plurality of 16-bit and 32-bit instructions being processed as 32-bit instructions. Support for these limitation are replete throughout Applicant's specification as filed.

As previously discussed, Applicant's invention requires no instruction translation of the type present in the prior art, thereby streamlining the architecture and operation of the core and

ISA. 16-bit instructions are processed as such, as are 32-bit instructions, and no translation between them is required, thereby further facilitating the "freeform" mixing of instructions described in Applicant's specification.

Applicant respectfully submits that none of the cited art used as the basis for the Examiner's rejection teaches or suggests such limitations in any way. Accordingly, the art cited by the Examiner cannot as a matter of law render Claim 26 as amended obvious, since not every limitation of the claim is present or suggested in such art.

Claim 40 - By this paper, Applicant has amended Claim 40 to include limitations relating to a majority of instruction opcodes being encoded within the top "n" bits, n being an integer greater than 1, the top n bits determining the format of the remaining bits within an instruction associated therewith. Support for these limitation are provided at, *inter alia*, page 17, lines 11-16 of Applicant's specification as filed.

Applicant respectfully submits that none of the cited art used as the basis for the Examiner's rejection teaches or suggests such limitations in any way. Accordingly, the art cited by the Examiner cannot as a matter of law render Claim 40 as amended obvious, since not every limitation of the claim is present or suggested in such art.

Claim 32 - By this paper, Applicant has amended Claim 32 to include limitations relating to (i) any immediate data fields in the compressed instruction set start from the least significant bit of respective ones of the instructions; and (ii) a plurality of instructions from the compressed instruction set each have at least one source register field located in common location therein. Support for these limitations are provided at, *inter alia*, page 17, lines 11-19 of Applicant's specification as filed.

Applicant respectfully submits that none of the cited art used as the basis for the Examiner's rejection teaches or suggests such limitations in any way. Accordingly, the art cited by the Examiner cannot as a matter of law render Claim 32 as amended obvious, since not every limitation of the claim is present or suggested in such art.

Claim 34 - By this paper, Applicant has amended Claim 34 to include limitations relating to only a subset of the recited available registers, and "implied" registers, being used by the recited compressed instruction, the subset and implied registers reducing the number of bits required to encode a register within the recited processor. Support for these limitations are provided at, *inter alia*, page 14, lines 6-15 of Applicant's specification as filed.

Applicant respectfully submits that none of the cited art used as the basis for the Examiner's rejection teaches or suggests such limitations in any way. Accordingly, the art cited by the Examiner cannot as a matter of law render Claim 34 as amended obvious, since not every limitation of the claim is present or suggested in such art.

New Claims

By this paper, Applicant has added new Claims 46-50, each of which are supported by the specification as filed. See, *inter alia*, pages 7-9 (referencing Figures 4-13 and 14-32) of Applicant's specification as filed regarding new Claims 48-50. Applicant submits that each of these new Claims distinguish over the art of record, and are also in condition for allowance.

Other Remarks

Applicant hereby specifically reserves all rights of appeal, and the right to prosecute claims of different or broader scope in a continuation or divisional application.

Applicant notes that any claim cancellations or additions made herein are made solely for the purposes of more clearly and particularly describing and claiming the invention. The Examiner should infer no (i) adoption of a position with respect to patentability, (ii) change in the Applicant's position with respect to any claim or subject matter of the invention, or (iii) acquiescence in any way to any position taken by the Examiner, based on such cancellations or additions.

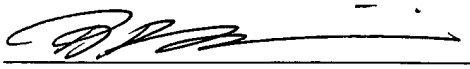
Furthermore, any remarks made with respect to a given claim or claims are limited solely to such claim or claims.

If the Examiner has any questions or comments that may be resolved over the telephone, she is requested to call the undersigned at (858) 675-1670.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

Dated: December 5, 2005

By: 

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